George Mason University

Department of Electrical and Computer Engineering

ECE 680 --- Physical VLSI Design Fall 2008

Homework 2 Due: Thursday, 10/2/2008

Policy: Provide details of the solution for each problem. A solution with only final results will not get credit.

Problem 1 - CMOS Inverter

> Use Microwind software to layout a CMOS inverter with L = 2 Lambda, W_n = 4 Lambda and W_p = 12 Lambda. Simulate the VTC and find the t_{pHL} and t_{pLH} of the inverter for the each of the three technology foundries: CMOS 0.12 µm, CMOS 0.18 µm and CMOS 0.25 µm. (Vdd = 2.5 V and f = 20 G Hz)

Problem 2 – sizing

Determine the sizes of the transistors in the complementary combination logic gate with function $F = \overline{D + A \cdot (B + C)}$ (the circuit was discussed in the class) such that it has approximate the same t_{pLH} and t_{pHL} as an inverter with the following sizes: NMOS: W/L = 0.5 µm / 0.25 µm and a PMOS: W/L = 1.5 µm / 0.25 µm. (Notice W_p/W_n is 3.)

Problem 3 – delay and pseudo-NMOS inverter

Given the choice between NOR or NAND logic, which one would you prefer for implementation in pseudo-NMOS. (Different with complementary logic gates we discuss in the class)

Problem 4

Implement the equation F =

$$((\overline{A} + \overline{B})\,(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G}$$

Using complementary CMOS. **Size the devices** so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6. Which **input patterns** would give the worst and best equivalent pull-up or pull-down resistance?